



SIMCom 5G Series Module PCIE USE NOTE

5G Module

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Document Title:	SIMCom 5G Series Module PCIE USE NOTE
Version:	1.00
Date:	2023-03-22
Status:	Draft version

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Version History

Date	Version	Description of change	Author
2023-03-22	V1.00	Draft version	Shaoxu.hou

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1 Introduction

1.1 Document introduction

This document describes design, debug and test notes of PCIE interface, with the help of this document, customers can quickly complete the design and analyze problems during debugging and testing.

1.2 5G module Models illustrate

The 5G series modules include many models, the model definition consists of these parts: module type, application scenario, processor platform, size of package, regional version and package type, for more details please reference figure below.

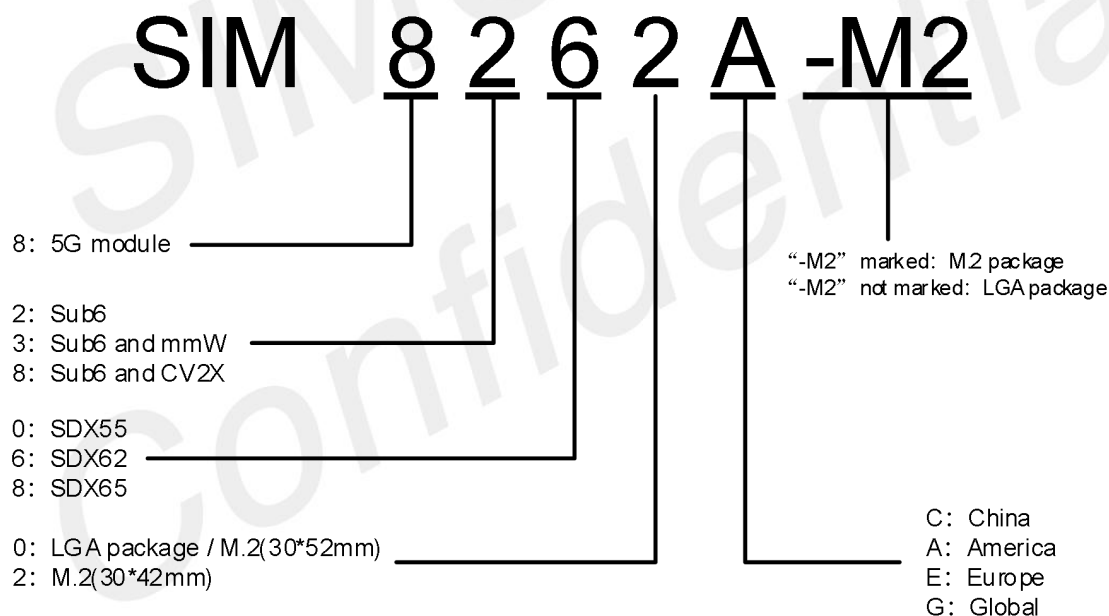


Figure 1: SIMCom 5G Module Model illustrate

2 Schematic NOTE

2.1 Note the location of AC capacitors and the connection direction of PCIE signals

All of the 5G modules contained AC capacitors in TX signals of PCIE, customers **only** need to connect AC capacitors at the TX signals of the external chip. Generally, the AC capacitors was suggested to close to TX signals pin side, it also can be placed anywhere in the PCIE signals.

The 5G module PCIE TX signals should be connected to RX signals of the external chip, the PCIE RX signals should be connected to TX signals of the external chip, the differential pair signals must Plus to Plus, Minus to Minus, avoid Plus connected to Minus. The placement location of AC capacitors and the connect direction of PCIE signals are shown in the following figure.

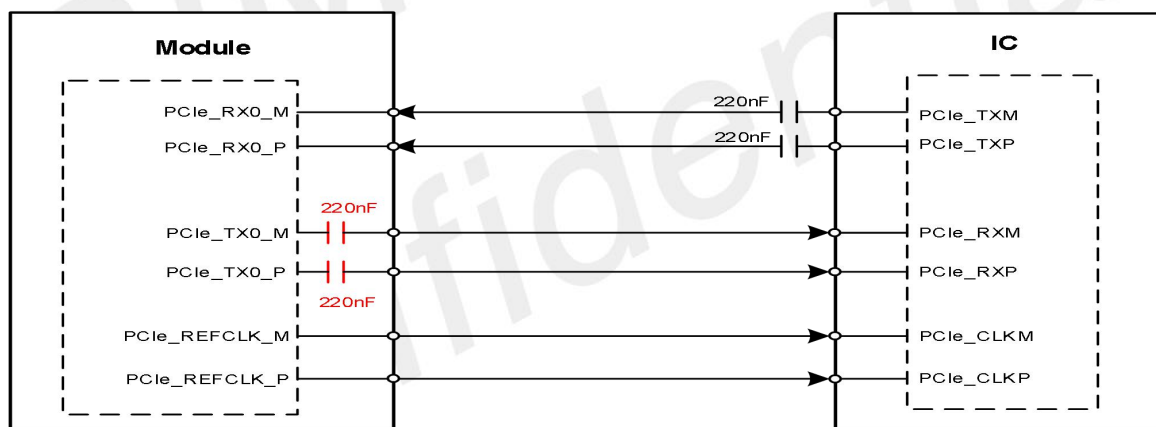


Figure 2: The placement location of AC capacitor and PCIE signals connect direction

The module support PCIE 3.0, the value of AC capacitors should be selected 176nF~265nF, 220nF was recommended, when the external chip which connected to module support PCIE 2.0, the value of AC capacitors should be selected 75nF~265nF, 100nF was recommended.

The AC capacitors is used to isolated the DC component and low-frequency noise, the different voltage domain can be used at both ends of AC capacitors, and prevent transient current during hot plug. The follow shows the waveform changes at the IC side before and after add the AC capacitors.

- If the module output VPP is a 1V square wave signal superimposed with a 1V DC signal, when there is no AC capacitor between module and IC, the waveform near the IC as bellow.

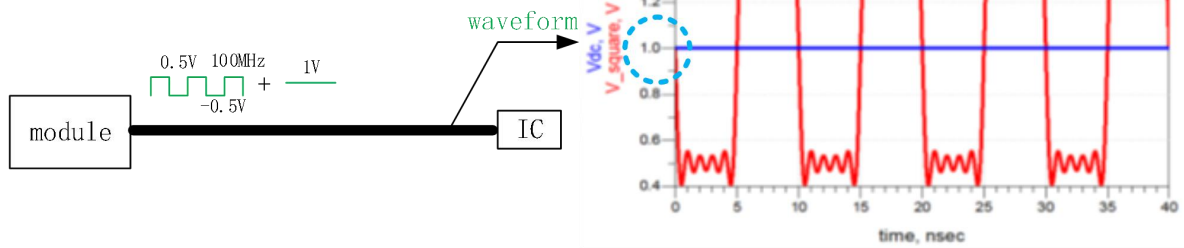


Figure 3: Module connect to IC without AC capacitor

- If the module output VPP is a 1V square wave signal superimposed with a 1V DC signal, there is an AC capacitor between module and IC, the waveform near the IC as bellow.

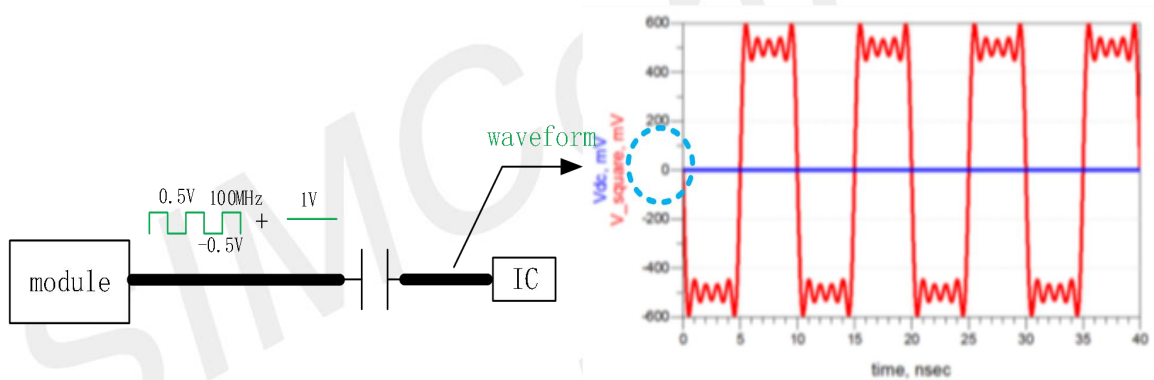


Figure 4: Module connect to IC with capacitor AC capacitor

- If the module output VPP is a 1V square wave signal superimposed with a 1V DC signal, there is an AC capacitor between module and IC, and the voltage domain of IC is 0.5V DC, the waveform near the IC as bellow.

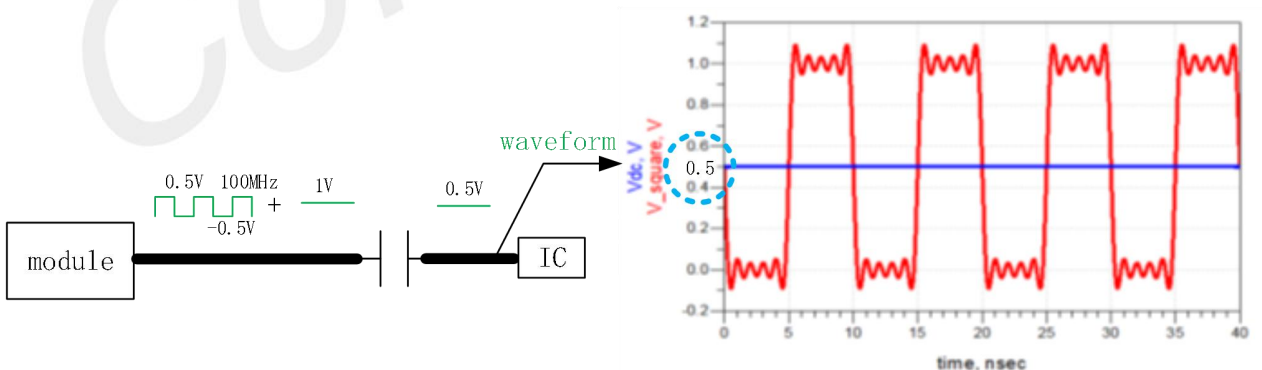


Figure 5: Module connect to IC with AC capacitor but different voltage domain

2.1.1 CASE1: The AC capacitors placement location error

The 5G modules has already include AC capacitors in TX signals, so customers should avoid place AC capacitors in TX signals outside the modules, the placement location of AC capacitors was error as follow figure shows.

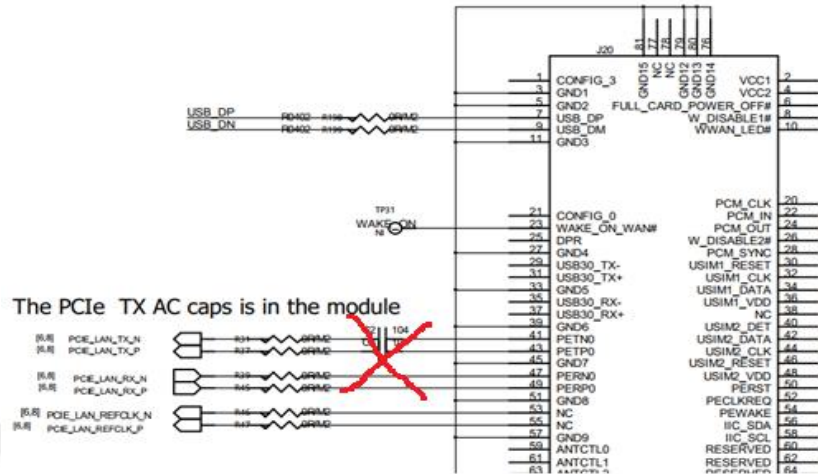


Figure 6: The placement location of AC capacitors error

2.2 Note place the TVS near M2 connector

All of M2 package module should place TVS on PCIE signals, the junction capacitance of TVS is less than 0.5 pf. The TVS should place near the M2 connector as close as possible.

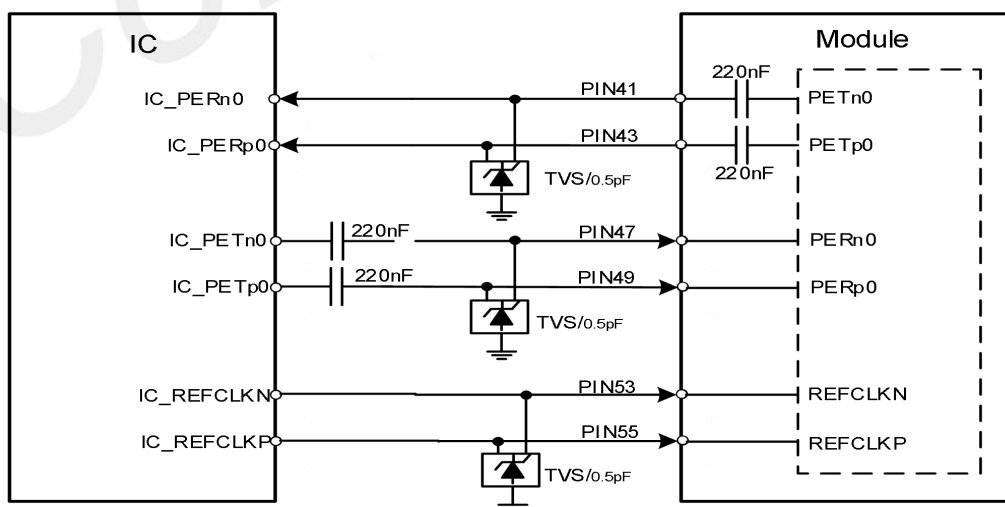


Figure 7: The M2 module should place TVS near M2 connector

2.3 Note the Level shift chip of PCIE auxiliary signal

The PCIE auxiliary signals include PCIE_WAKE, PCIE_RESET and PCIE_CLKREQ. Customers should note the voltage domain of PCIE auxiliary signals.

For all of the M2 modules, the voltage domain of PCIE auxiliary signals are 3.3V. If customers need 1.8V voltage domain, the M2 module need to be customized.

For all of the LGA modules, the voltage domain of PCIE auxiliary signals are 1.8V. In customer's design, if the voltage domain is not 1.8V, customers need to add level shift circuit.

The PCIE signals of PCIE_WAKE and PCIE_CLKREQ need to add 4.7K Ω pull up resistors. It is recommended to reserve 4.7K Ω pull-up resistors at both side of the level shift chip. The recommended level shift circuit as follow figure shows.

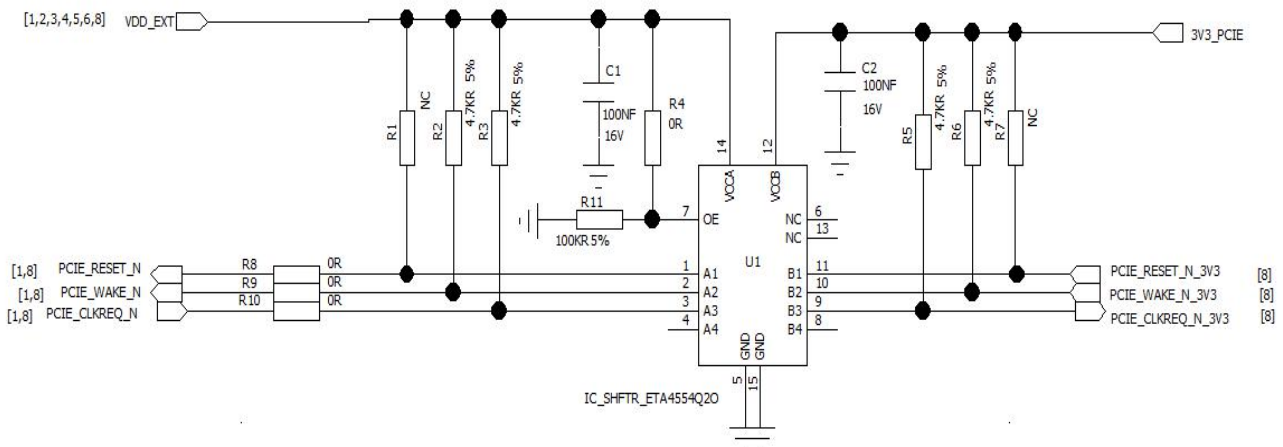


Figure 8: Level shift chip circuit example

The normal waveform of PCIE auxiliary signals before and after level shift chip were shown in the following figure:



Figure 9: The normal waveform of PCIE auxiliary signals (1.8V and 3.3V voltage domain)

Pay special attention to the OE pin of the level shift chip, if customer want use the internal pull-up resistors of level shift chip. The OE pin of level shift chip may high active or low active. When customer selected the level shift chip which the OE pin is high active, if the VCCA is not power on, the OE pin is low, the level shift chip can't be enable and the internal pulled up resistors internal of level shift chip will can't work.

Customer should avoid to select the level shift chip which the OE pin is low active.

The PCIE_CLKREQ is used for hardware Active State Power Management (ASPM), active low. The PCIE_CLKREQ signal is power save function by hardware. When the PCIE_CLKREQ was low level (lower than 1.0V, 1.8V voltage domain), the PCIE_REFCLK of module will start the REFCLK signal, the PCIE_REFCLK will open all the time. If the PCIE_CLKREQ was high level (higher than 1.2V, 1.8V voltage domain), the module will end the PCIE_REFCLK.

The waveform of PCIE_CLKREQ and PCIE_REFCLK is showed as follow figure.

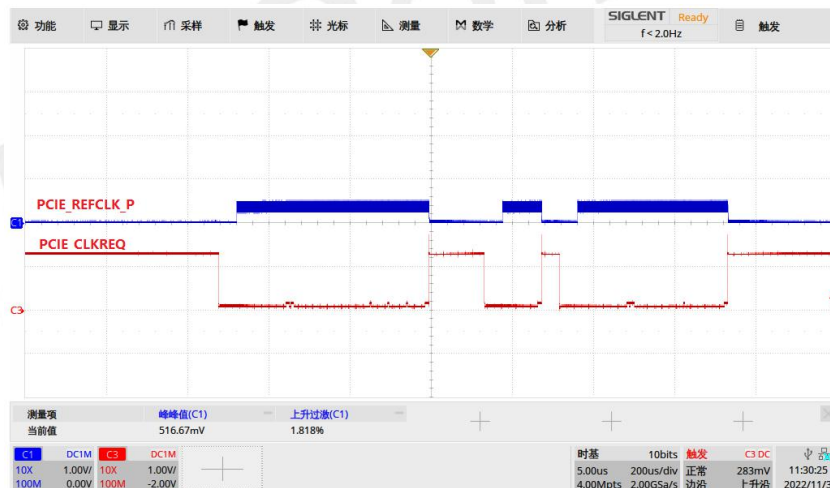


Figure 10: The PCIE_CLKREQ and PCIE_REFCLK signals waveform

The PCIE_CLKREQ signal is input signal in RC mode and output signal in EP mode for 5G module.

The PCIE_RESET signal is used for module reset the external chip or the external chip reset the module, active low. The follow figure shows the PCIE_RESET and PCIE_REFCLK signals power-on sequence when the module is in RC mode.

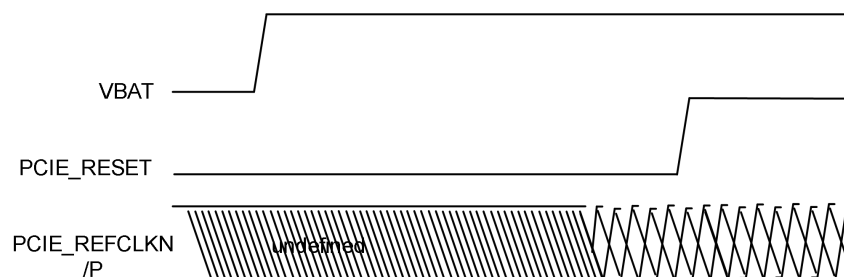


Figure 11: PCIE_RESET and PCIE_REFCLK signals power-on sequence

The PCIE_WAKE signal is used for wakeup, active low.

The PCIE_WAKE signal is input signal in RC mode and output signal in EP mode.

In RC mode, when the PCIE_WAKE signal is low level, the external chip will wake up the module. The follow figure shows the PCIE_WAKE signal changed when the PCIE_WAKE signal has worked.

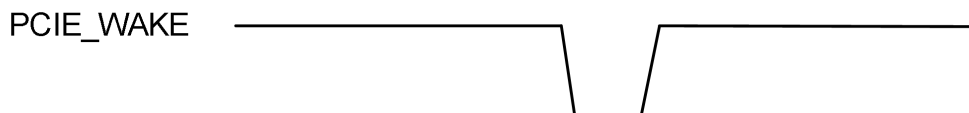


Figure 12: The waveform of PCIE_WAKE signal

2.3.1 CASE1: The PCIE auxiliary signals voltage domain connect error

In compatible design, PCIe auxiliary signals should make sure the voltage domain was correct before and after the level shift chip, if the PCIe auxiliary signals connected the incorrect voltage domain, the function of PCIe can't work normally.

As the follow figure shows, customer made a compatible design on PCIE auxiliary signals for M2 module and LGA module, the BB_PCIE nets are connected to LGA module, the M2_PCIE_LAN nets are connected to M2 module.

When customer used the LGA module, there is no problem. But when customer used M2 module, as the red square shows, the voltage domain of PCIE auxiliary signals is 3.3V, but they were wrongly connected to the 1.8V voltage domain, so the external chip which connected to the module can't work normally.

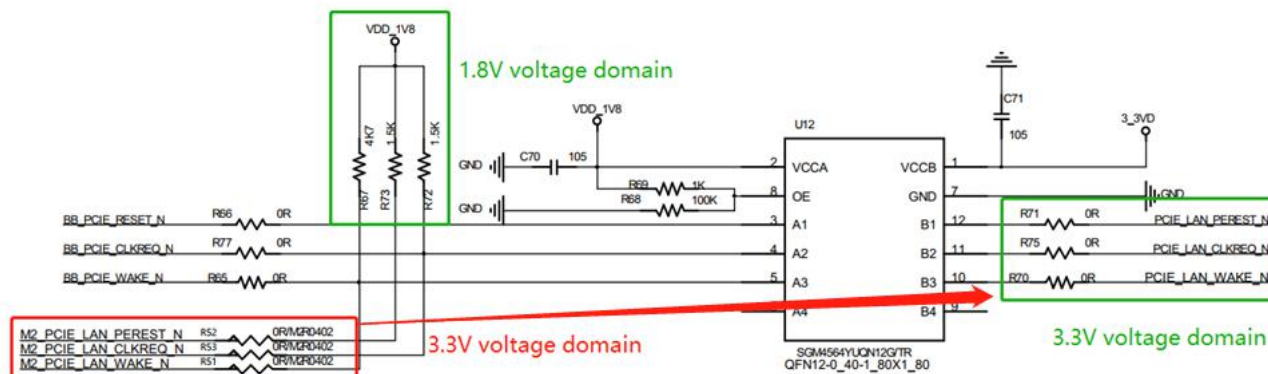


Figure 13: The voltage domain of PCIe auxiliary signals connect error

The same signal should connect together. The signals in red square should connect to the 3.3V voltage domain of the green square as figure shown above. The follow simplified diagram was shown the correct connection of PCIE auxiliary signals.

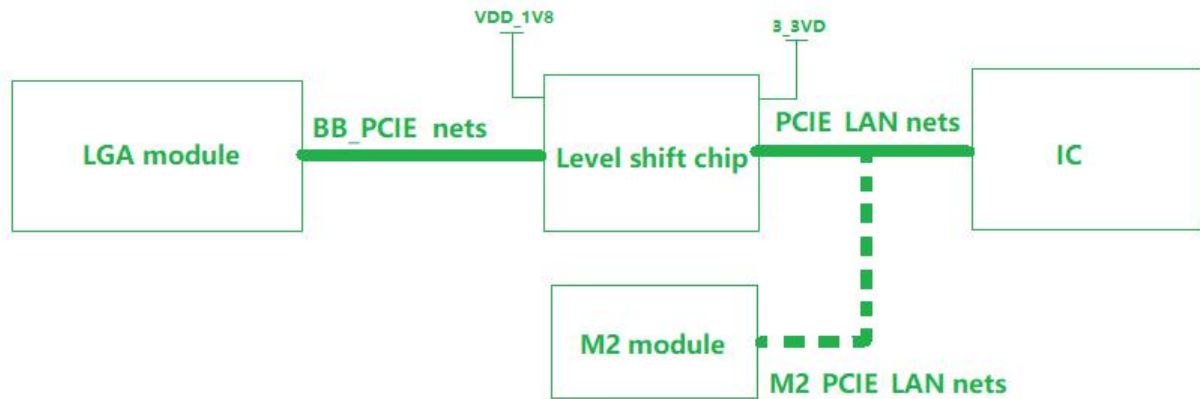


Figure 14: The voltage domain of PCIE auxiliary signals connect correct

2.3.2 CASE2: RTL8125B PHY can't be recognized by missed pull up resistor

The RTL8125B PHY can't be recognized by module. Customer used a level shift chip which model is LSF0204RGYR, this level shift chip used for open-drain and push-pull applications.

As the follow level shift circuit shows, on RTL8125B side, the high level of reset signal is above 2V (3.3V voltage domain), because there are no pull up resistor at both sides of level shift chip, and level shift chip don't has pull up resistors internally, so the RTL8125B recognized the RESET signal is always low level, the module can't pull up it to above 2V and can't initialize it.

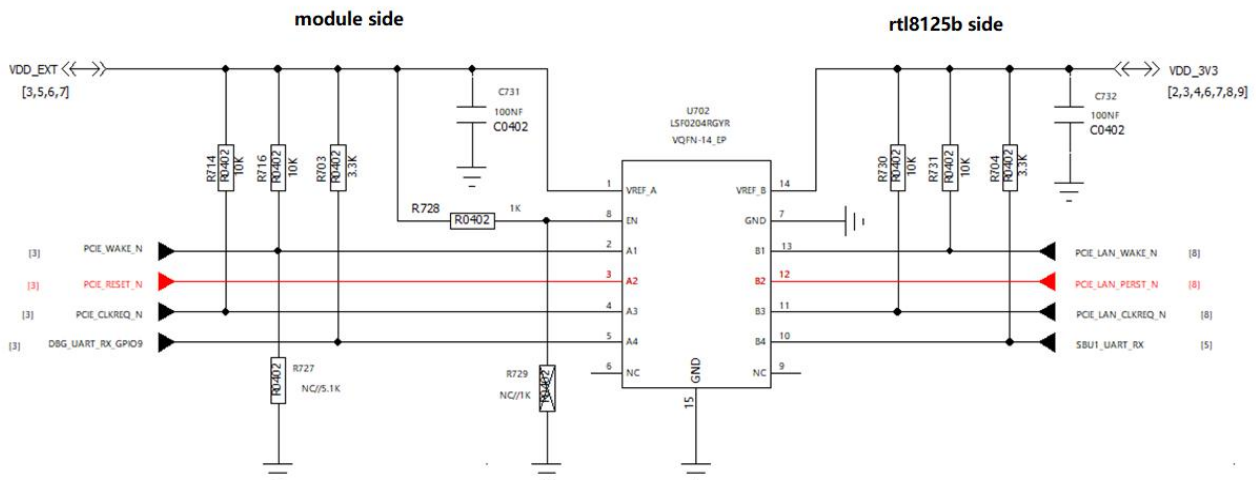


Figure 15: The RTL8125B PHY side miss add pull up resistor

Customer should add 4.7KR pull up resistors at the RTL8125B side.

3 PCB NOTE

3.1 Note the impedance of differential pairs

The PCIE_RX0_P/M, PCIE_RX1_P/M, PCIE_TX0_P/M, PCIE_TX1_P/M, PCIE_REFCLK_P/M traces must control 85 ohm differential impedance. According to the stacked structure of the board, customers should calculate the impedance through the Polar Si9000 or other software.

The follow figure shows the impedance of differential pair calculation with Si9000.

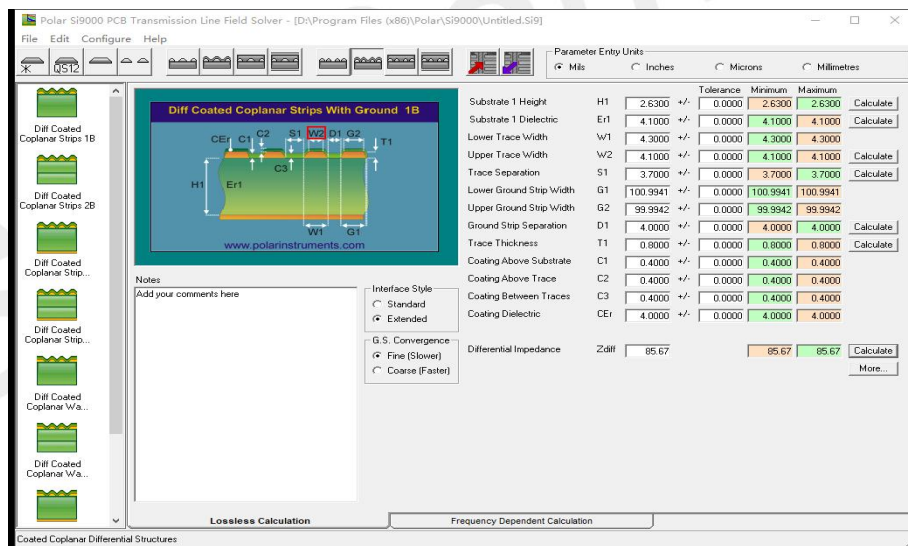


Figure 16: The calculation results of impedance

Impedance mismatch will produce reflections, and the reflection will cause overshoot, ringing, and jitter, and it will cause the slope of rising edge or falling edge to become slowly. The follow figure shows the impedance mismatch caused overshoot and ringing.

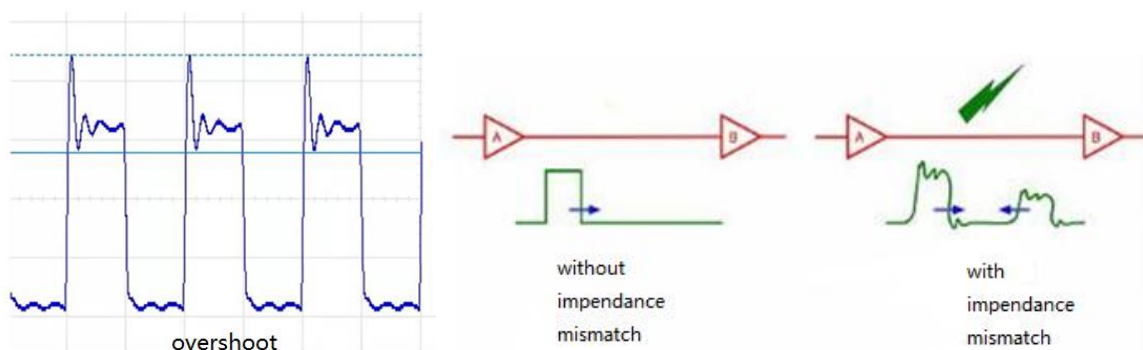


Figure 17: Impedance mismatch caused overshoot and ringing

3.2 Note the length of PCIE signals in PCB

The traces length between the PCIE pins of CPU and the external chip, the shorter the better.

The longer traces may cause larger distributed inductance and distributed capacitance, which will have a lot of influence on the high-frequency signal of the system, and will also change the characteristic impedance of the circuit, resulting in reflection and oscillation of the system.

The total trace length is less than **150mm**. For most LGA module, the trace length in module is about **30mm**, so the trace length from module to customer's design is less than **120mm**. For most M2 module, the trace length in module is about **10mm**, so the trace length from module to customer's design is less than **140mm**.

The mismatch between the lengths of the two traces in the differential pair should be less than **0.5mm**. The follow figure shows the total length and the mismatch of PCIE.

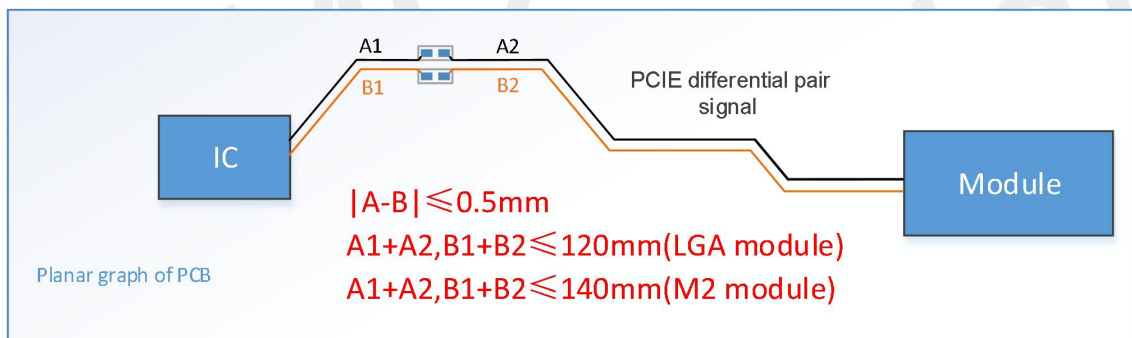


Figure 18: The total length and the mismatch of PCIE

The differential pair signal mismatch will case common-mode interference and jitter of the eye diagram. Normally, the differential pair signal is matched, the common-mode component is zero or DC component. If the differential pair signal is mismatched, it will caused the transmission time inconsistency and caused the common-mode interference. The follow figure shows the common-mode component which differential pair is matched and mismatched.

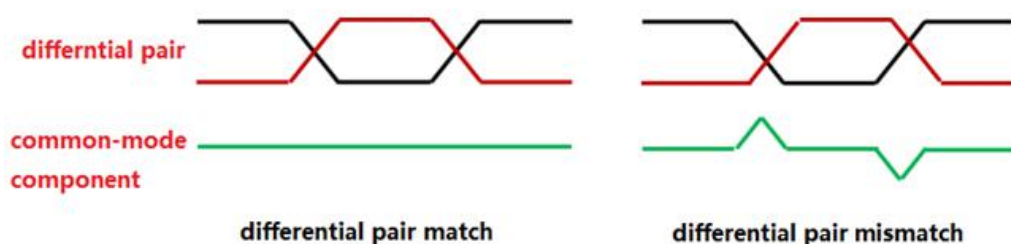


Figure 19: The mismatch caused common-mode component diagrammatic drawing

3.2.1 CASE1: The PCIE signals layout length more than 150mm

As the follow layout figure shows, the trace length of PCIE signals on the board is more than 130mm, the length of other board which connected to BTB connector is more than 30mm, so the total trace length is more than 150mm.

Customers should calculate the total length of the most length trace of PCIE, make sure the total length of the most length trace of PCIE is less than 150mm.

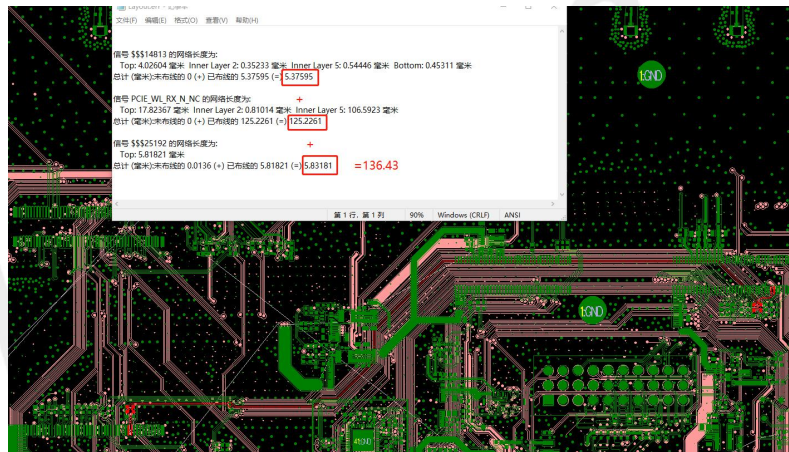


Figure 20: The PCIE signals layout length more than 150mm

3.2.2 CASE2: The mismatch length between the two traces more than 0.5mm

The follow figure shows the two traces length which is one differential pair, the mismatch length is about 1mm, it is more than more than 0.5mm, customers should avoid the mismatch length between the PCIE differential pair is more than 0.5mm.

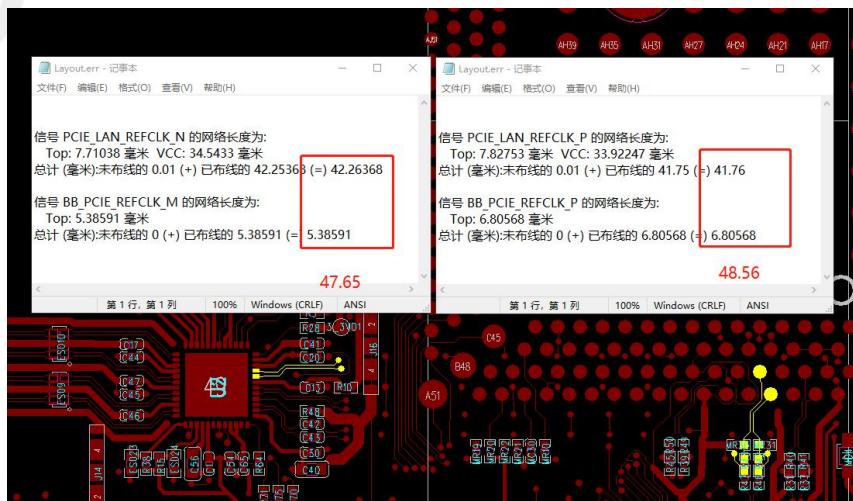


Figure 21: The differential pair length mismatch more than 0.5mm.

3.3 Note the trace space of PCIE signals

The trace space between each differential pairs of PCIE and between other signal traces should not be less than 4 times the trace width.

The follow figure shows the space between the differential pair of PCIE on cutaway view of PCB.

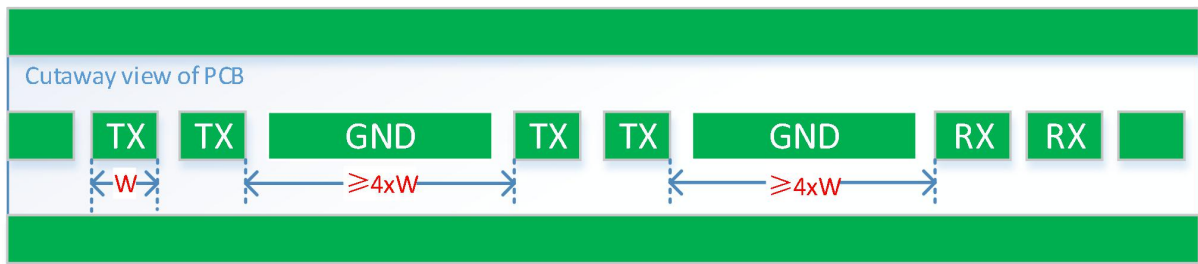


Figure 22: The space between differential pair of PCIE

If the space between PCIE signals and other signals is not enough, and too small spacing may cause crosstalk between adjacent signals. The follow figure shows the waveform of the crosstalk caused by PCIE signals and other signals too small.

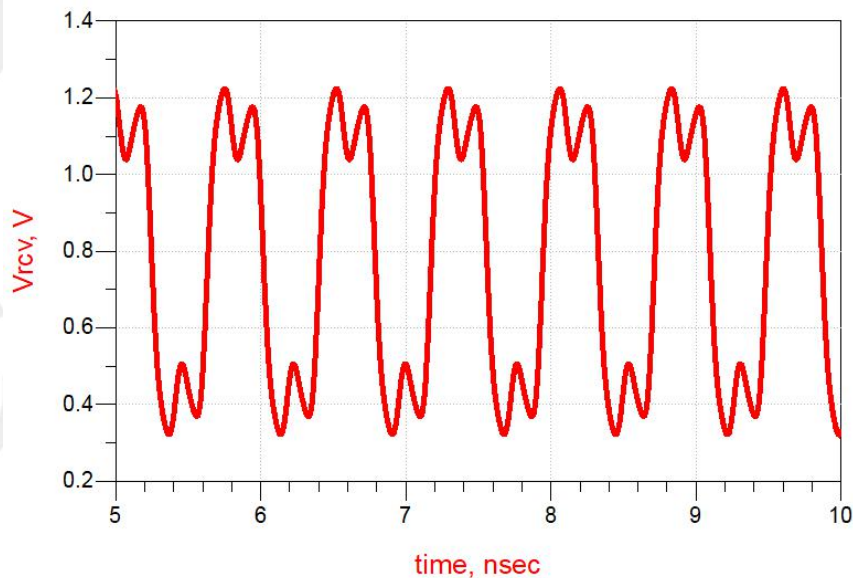


Figure 23: The waveform of crosstalk example

3.4 Note the placement and location of AC capacitors in PCIE signals

The two AC capacitors in the same differential pair should be placed close to each other. The follow figure shows the placement of AC capacitors in the same differential pair.

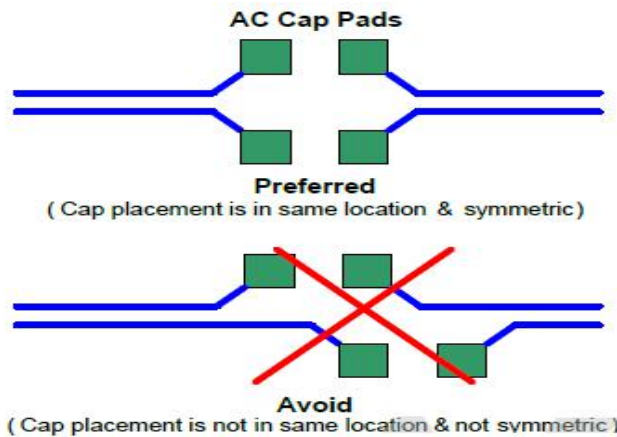


Figure 24: The placement of AC capacitors in PCIE trace

The AC capacitor which on the TX signals of IC was suggested to close to TX signals pin side. The follow figure shows the location of AC capacitors.

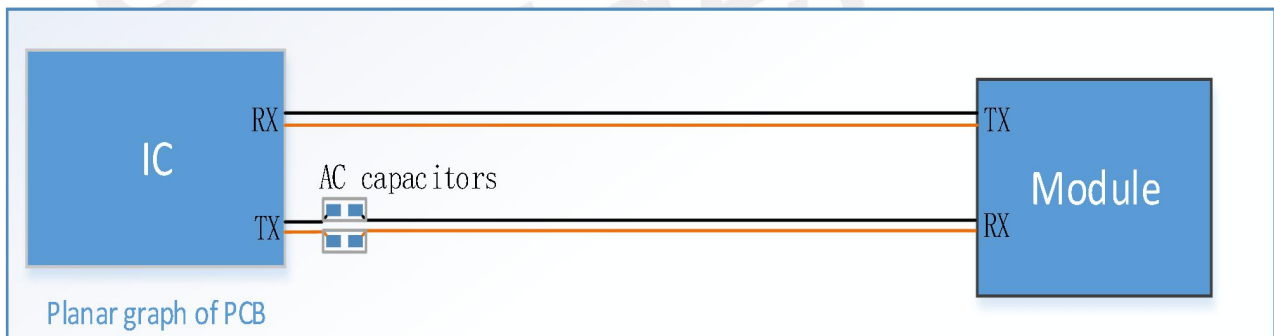


Figure 25: The AC capacitors location near output

3.5 Note the via and test pad placement location on PCIE signals

When the PCIE signal change layer, the GND via should be placed close to the signal via, and one to three GND via are recommended for each pair of signals, too many signals via will caused the insertion loss of the PCIE signal high and may limit the maximum trace length, up to four pairs via can be used in TX differential pairs and up to two pairs via can be used in RX differential pairs.

The out circle of via is less than 25mil and the inner circle of via is less than 14 mil, and the two via must be placed close to each other.

If customers placed the test pad on the PCIE signals, make sure the test pad should as small as possible and avoid caused stub. The placement location of PCIE signal via and test pad as follow figure.

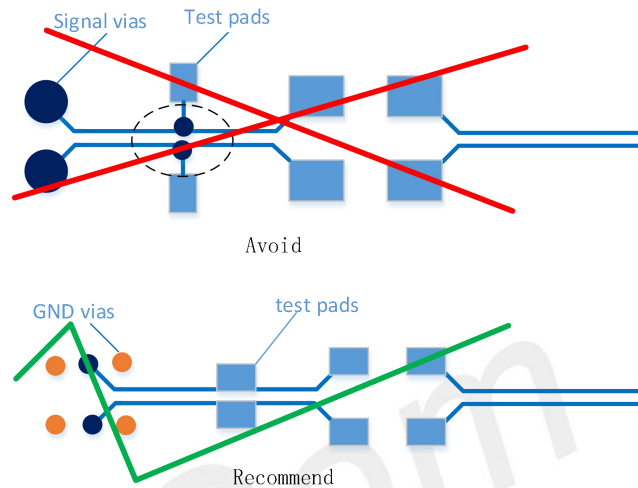


Figure 26: The signal via and test pad placement location on PCIE signals

3.6 Note the differential pair signals of PCIE surround by GND

The differential pair signals of PCIE should be routed on the inner layer as much as possible, all of PCIE signals should be surround by GND well and on both sides of differential pair signals should also be surround by GND.

On the both side differential pair signals should place GND via. Note the distance of GND via, when the distance of GND via is about 1/10 of the wavelength corresponding to the signal's highest frequency, the reflected oscillation caused can be basically cancelled. The follow figure shows the differential pair signals of PCIE were surrounded by GND.

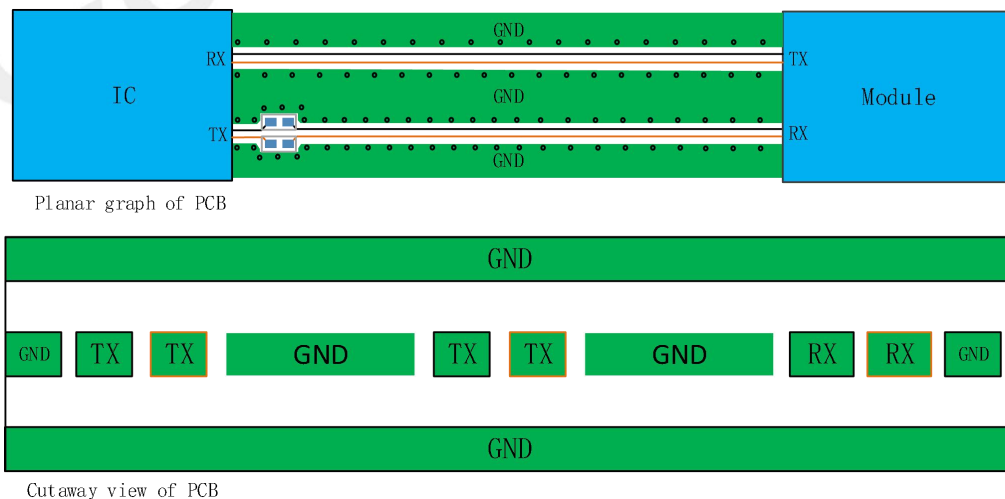


Figure 27: Differential pair signals of PCIE surround by GND

3.6.1 CASE1: The PCIE signals trace surrounded by GND is incomplete

The follow figure shows the layout of RTL8125B and module, the communication between module and RTL8125B is PCIE. The PCIE signals trace which on RTL8125B side and module side were surrounded by GND incomplete. The trace length which from pin out without surrounded by GND should less than 50mil.

The figure shows the trace of PCIE signals which connected to RTL8125B and module was surrounded is incomplete.

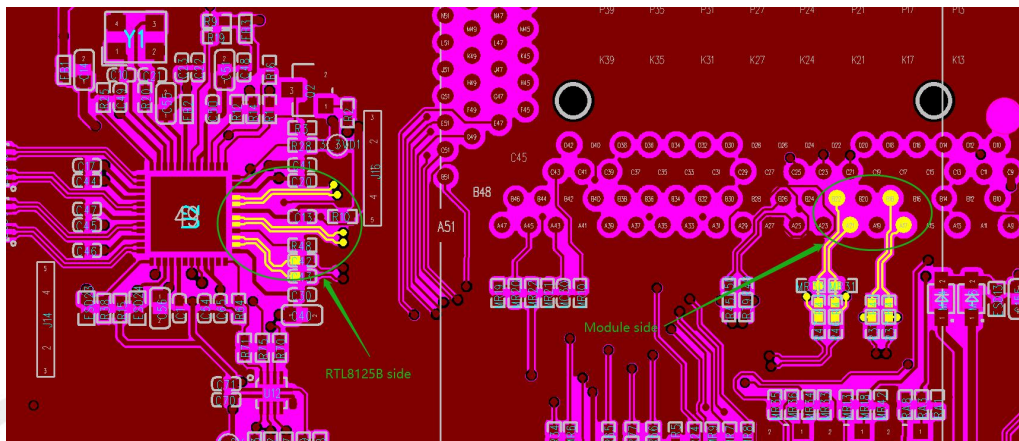


Figure 28: PCIE signals trace were surrounded by GND incomplete

3.6.2 CASE2: E-pad of RTL8125B PHY was not solder mask open

The E-pad of RTL8125B is the Analog and Digital Ground, it is the main GND of RTL8125B, and it is also used to heat dissipation.

If the E-pad not connect to GND enough, the communication speed of RTL8125B may not up to 1Gbps. Customers should avoid to place the large via on the E-pad of RTL8125B. The E-pad of RTL8125B need solder mask open to increase the area connected to GND and help to heat dissipation. The follow figure shows the E-pad of RTL8125B was not solder mask open.

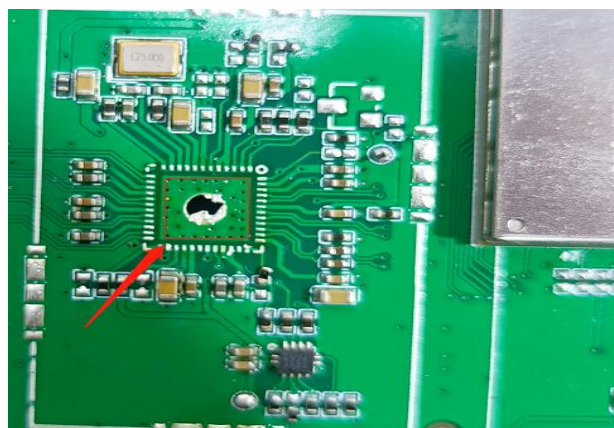


Figure 29: The E-pad of RTL8125B not solder mask open

3.7 Note the continuity of PCIE signals reference plane

PCIE signals should have a complete reference plane, avoid discontinuities in the reference plane, such as splits and voids. The following figures show the reference plane of PCIE signals is not continuity.

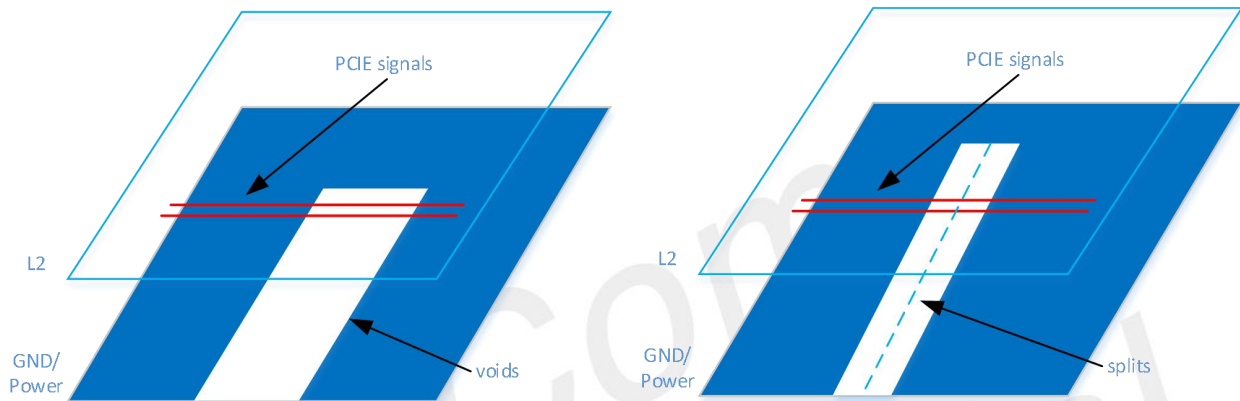


Figure 30: The reference plane should avoid splits and voids

3.8 Note the PCIE signals keep away from strong interference signals

PCIE signals should keep away from strong interference signals such as RF, clock, crystal oscillator and high power supply.

3.9 Note the layout of the PCIE signals avoid forks

The layout of PCIE should avoid to form branch or stub. Stubs have a large impact on impedance and can cause signal reflection and overshoot, so customers should usually avoid stubs and branches when designing.

The influence on the signal is reduced by means of Daisy chain routing.

The following figures show the simple graph and PCB layout of PCIE signals forks.

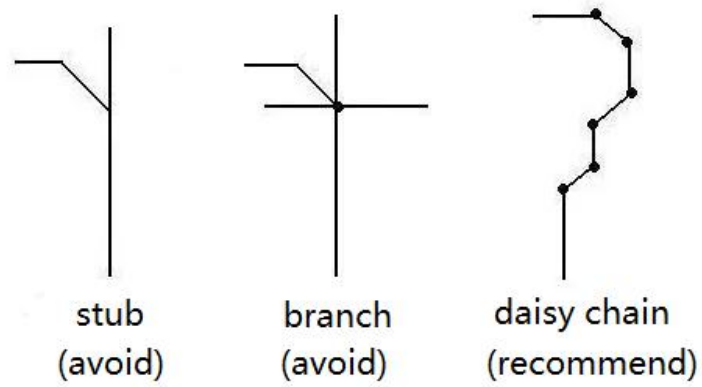


Figure 31: The simple graph of PCIE signals forks

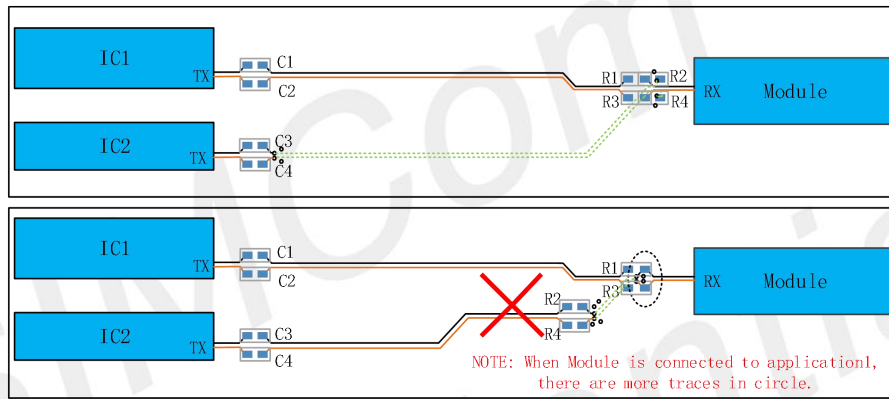


Figure 32: The PCB layout of PCIE signals forks